ABSTRACT

Methods and apparatus are disclosed for reducing power consumption and complexity when performing Forward Error Correction (FEC) through parallel decoding techniques. In particular, techniques are described for reducing power consumption and complexity of Reed-Solomon (RS) FEC decoding that is performed in a parallel manner. Steps are taken to reduce power consumption in a FEC decoder when an actual number of errors is less than a maximum error correction capability of the FEC code and when there are no errors. Power is also reduced through limiting hardware complexity of a parallel implementation of a FEC decoder. Hardware sharing is used to reduce overall complexity. A low complexity scheme is used to determine uncorrectable errors in an example RS(255,239) code. In addition, a low complexity encoder is disclosed that converts input symbols to an appropriate format for a particular symbol encoding technique.